A Design Method of Burn-in for AD/DA Converter Based on Integrated Circuit Architecture

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Abstract: Based on the research of circuit function module and Architecture, this paper establishes the relationship between failure mechanism and failure mode of AD/DA Converter, and proposes a dynamic burn-in design method of AD/DA converter based on circuit architecture. The analysis shows that the dynamic burn-in pattern designed by this method is simpler to implement, and the dynamic burn-in coverage and switch flip rate are significantly improved, which improves the effectiveness of dynamic burn-in. The proposed burn-in design method has good versatility and can be applied to the dynamic burn-in design of various functions integrated circuits. This method has broad application prospects.

1. Introduction

The analog-to-digital/digital-to-analog converter (AD/DA converter) circuit is an indispensable module in electronic systems and can be applied to aerospace high-reliability systems, including measurement and control, communication, guidance, navigation and control (GNC), information management and power division system. Therefore, the research on the quality of AD/DA converters used in the aerospace field is very important.

As an important part of the quality assurance of AD/DA converter, the Burn-in is an effective means to eliminate the defects introduced by manufacturing and application process. It is inevitable that AD/DA converters have defects, so that the reliability of the devices cannot meet the requirements. Burn-in can activate these potential defects and remove defective devices before used [1]. Burn-in can mainly expose time-and-stress-related failures, and it is a combination of various stresses such as electrical stress (voltage or power) or thermal stress. These stresses can accelerate the physical and chemical reactions inside the devices, activating and exposing potential defects. Therefore, early-failure and barely-qualified devices could be rejected [2].

2. Relationship between typical circuit failure mechanism and failure mode

The development of integrated circuit technology has brought higher operating frequency and smaller chip size. It has also caused the negative impact of thinner metal interconnect lines and gate oxide thickness. So the minor defect, that did not affect the life of integrated circuits in the past, have a major impact on their reliability. That the integrated circuit is not affected in the past. Small defects in service life also have a major impact on their reliability. After the characteristic size of the integrated circuit was reduced to deep submicron, the gate dielectric breakdown (TDDB), hot carrier injection(HCI), negative bias temperature instability(NBTI) and electro migration(EM) became the main failure mechanism [3, 4].

Taking the typical successive approximation AD converter (SAR ADC) as an example, the intrinsic relationship between the failure mechanism and function degradation of integrated circuits are analyzed. Figure 1 shows core module block diagram of a SAR ADC.

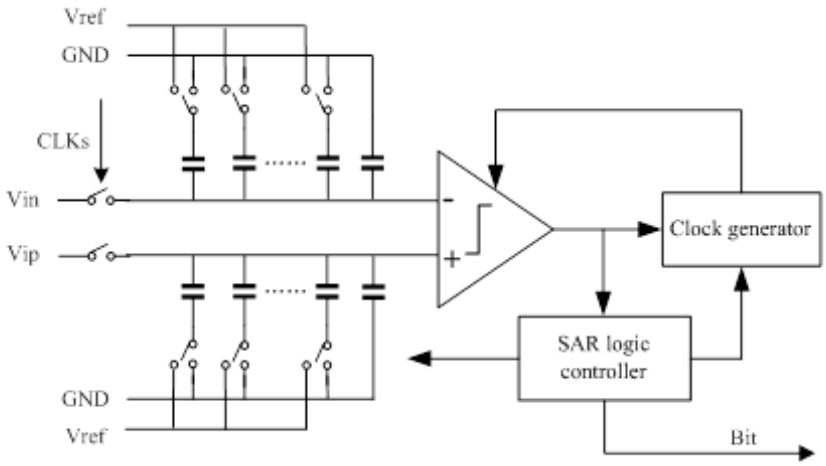

Fig. 1 The typical architecture of SAR ADC

The TDDB will cause the SAR ADC power consumption and leakage to exceed the specification. In addition, if the TDDB phenomenon occurs in the SAR ADC front-end sample-and-hold module, it will affect its resolution. The HCI effect will cause the threshold voltage of the MOS FET drift or Trans conductance decrease. The HCI effect has a great influence on the comparator and output unit of the SAR ADC, which will cause the device offset error and the gain error. The NBTI effect causes the threshold voltage and signal delay of the MOS FET to increase and the drive current to decrease. Therefore, this effect has an influence on the digital SAR logic controller in the ADC, which will cause control logic errors and delay increase, resulting in an abnormal conversion rate and even causing functional failure. The electro migration The EM effect is more pronounced when the circuit size continues to decrease. It would increase the failure probability of the metal wire, causing logic errors or even functional failures of the SAR ADC.

3. The Burn-in Pattern of AD/DA Converter Based on Circuit Architecture

The ideal burn-in pattern should make all transistors inside the converter to be 100% upside down. In this state, all potential defects on the chip are effectively excited by the electrical stress. The design of the burn-in pattern should be based on the principle of simplicity and practicality. It does not pursue the complexity of the function, but enhances the coverage as much as possible.

Unlike FPGA or other types of VLSI, the AD/DA converters have relatively simple circuit structure and function. It is not difficult to design a burn-in pattern of high coverage rate. As long as focus on the setting of the enable signal of different functional modules in the converter and increasing of the digital module switch toggle rate, a full-coverage and high-toggle-rate burn-in pattern should be designed.

When designing AD/DA converter burn-in pattern, we should base on the circuit structure to set the external input clock signal frequency and waveform. The internal components of the AD/DA converter are subjected to as much electrical stress as possible to more effectively excite defects in the circuit.

3.1 The Burn-in Pattern of FLASH ADC

When we design dynamic burn-in pattern for an ADC based FLASH architecture, the input signal of ADC should be set to be sinusoid, in order to make the burn-in coverage of each comparator more comprehensive and make thermometer decoder flip at higher frequency.

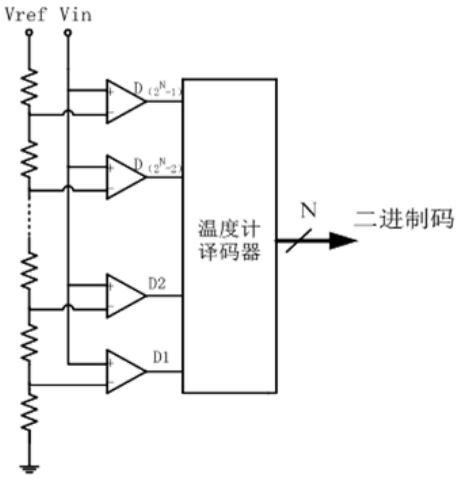

Fig. 2 structure diagram of FLASH ADC

3.2 The Burn-in Pattern of SAR and other architecture ADC

In addition to the FLASH architecture, the SAR ADC, the pipeline ADC [5] and the distributed ADC all include a sub-DAC module, and this module is the core module in the ADC circuit. The burn-in pattern is set with special consideration for the working mode of the module. The sub-DAC modules of these three types ADCs are generally composed of a binary capacitor array and a switch array. In order to make the switch array have a higher flip rate, the dynamic burn-in pattern can be set to a square wave signal with a duty ratio of 50%. .

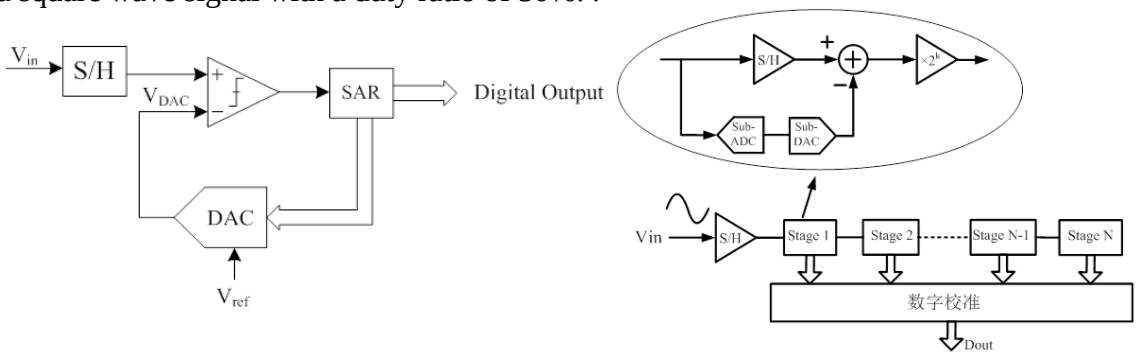

Fig. 3 structure diagram of SAR ADC and Pipeline ADC

3.3 The Burn-in Pattern of Voltage-based DAC

In a voltage-based DAC, the different input digital codes correspond to the state of the internal decoder and 2N switches, that is, each different input digital code will control the corresponding switch to be closed or open state. Therefore, when designing the voltage-based DAC burn-in pattern, all input conditions should be considered. The input waveform can be a signal that is incremented or decremented sequentially from 00...00 to 11...11 or 11...11 to 00...00. The pattern digital code can be obtained by dividing the 50% duty cycle square wave signal by the frequency divider multiple times.

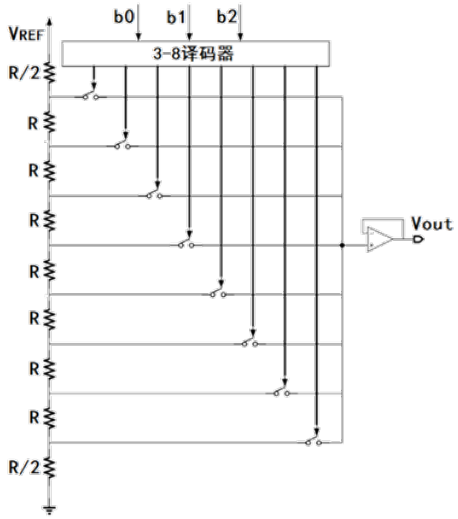

Fig. 4 structure diagram of Voltage-based DAC

3.4 The Burn-in Pattern of Charge-based and Current-based DAC

The charge-based DAC is similar to the current-based DAC, which contains a capacitor array and current array in multiples of 2. When the input digital code is 00...00, the switches in each branch of the circuit are disconnected, and when the input digital code is 11...11, the switches in each branch of the circuit are closed. Therefore, the burn-in pattern of these two architectures DAC should be 50% duty cycle square wave, and the internal switches of the device would have higher flip coverage during the burn-in.

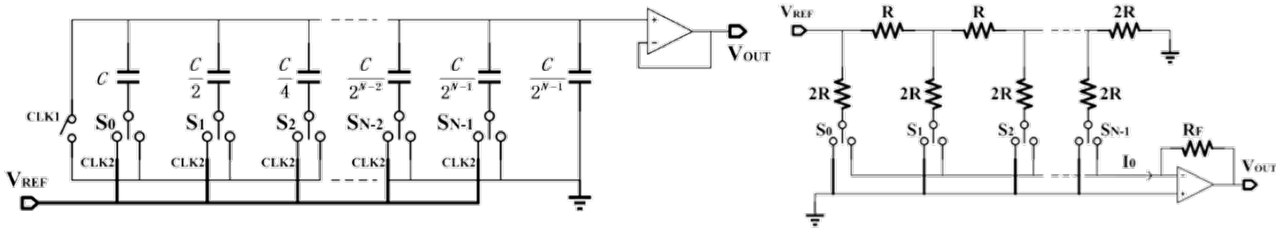

Fig. 5 structure diagram of Charge-based and Current-based DAC

4. Conclusion

This paper proposes a design method of AD/DA Converter burn-in. The method is based on the analysis of circuit architecture. The burn-in pattern with this method could have a high coverage and switching flip rate. The paper studies and analyzes the internal relationship between failure mechanism of the transistor and failure mode of the circuit. The research results provide theoretical basis for the design of the burn-in. The research shows that the design method of the burn-in for the AD/DA converters of different architectures can effectively improve the effectiveness and coverage of the burn-in pattern.

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